

Multicore Computer Architecture - Storage and Interconnects

Tutorial 1B

Instruction Pipeline & Performance



NPTEL Online Course : Multi-Core Computer Architecture and Interconnects Dr. John Jose, IIT Guwahati

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Tutorial Problem-1

- ❖ A company is releasing 3 modification versions of its processor architecture. The modifications that are being considered have multiple ramifications to the three major components (X, Y and Z) of the processor. The ramifications are outlined in the following table, in which each entry denotes the factor by which the speedup of that component in the column header will be affected. The fractions of the total execution time for the three components, X, Y, and Z are 30%, 45%, and 25%, respectively, identify the speedups (or slow down) that are to be expected from each of these 3 modification versions. Rank the three modifications in terms of speedup.

Version	X	Y	Z
A	1.4	0.8	1.5
B	0.6	1.6	1.8
C	1.3	1.4	0.9

Tutorial Problem-1

Version	X (30%)	Y (45%)	Z (25%)
A	1.4	0.8	1.5
B	0.6	1.6	1.8
C	1.3	1.4	0.9

Tutorial Problem-2

- ❖ Assume that the original machine is a 5-stage pipeline with a 1ns clock cycle. The second machine is a 12-stage pipeline with 0.6ns clock cycle. The 5-stage pipeline experiences a stall due to a data hazard for every 5 instructions, whereas the 12-stage pipeline experiences 3 stalls for every 8 instructions. In addition, branches constitute 20% of the instructions, and the mis-prediction rate for both machines is 5%. If the branch misprediction penalty for the first machine is 2 cycles but the second machine is 5 cycles, What is the speedup of the 12-stage pipeline over the 5-stage pipeline, taking into account (a) only data hazards (b) both data hazard and mis-prediction.

Tutorial Problem-2

- ❖ 5-stage pipeline (1ns cc). 6 cycles / 5 instruction + 2 cycles for branch
- ❖ 2-stage pipeline (0.6ns cc). 11 cycles / 8instructions+ 5 cycles for branch.
- ❖ 20 % branches with 5% mis prediction.

(a) only data hazards (b) both data hazard and mis-prediction.

Tutorial Problem-3

- ❖ Assume a standard 5 stage pipeline (IF-ID-EXE-MEM-WB), how many cycles it will take for the following code to get complete in a normal pipeline (a) without using operand forwarding { Format: Opcode Destn, Src1, Src2}

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ADD	R1,R2,R3															
SUB	R4,R1,R5															
AND	R6,R1,R7															
OR	R8,R1,R9															

Tutorial Problem-3

- ❖ Assume a standard 5 stage pipeline (IF-ID-EXE-MEM-WB), how many cycles it will take for the following code to get complete in a normal pipeline (b) with operand forwarding. { Format: Opcode Destn, Src1, Src2}

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ADD	R1,R2,R3															
SUB	R4,R1,R5															
AND	R6,R1,R7															
OR	R8,R1,R9															

Tutorial Problem-3

- ❖ Assume a standard 5 stage pipeline (IF-ID-EXE-MEM-WB), how many cycles it will take for the following code to get complete in a normal pipeline (a) without using operand forwarding
{Format: Opcode Destn, Src1, Src2}

[illegible]

Tutorial Problem-3

- ❖ Assume a standard 5 stage pipeline (IF-ID-EXE-MEM-WB), how many cycles it will take for the following code to get complete in a normal pipeline (b) with operand forwarding. { Format: Opcode Destn, Src1, Src2}

[illegible]

Tutorial Problem-3

- ❖ Assume a standard 5 stage pipeline (IF-ID-EXE-MEM-WB), how many cycles it will take for the following code to get complete in a normal pipeline (a) without using operand forwarding
{ Format: Opcode Destn, Src1, Src2}

[illegible]

Tutorial Problem-3

- ❖ Assume a standard 5 stage pipeline (IF-ID-EXE-MEM-WB), how many cycles it will take for the following code to get complete in a normal pipeline (b) with operand forwarding. { Format: Opcode Destn, Src1, Src2}

[illegible]

Tutorial Problem-4

- ❖ Consider the following instruction sequence executed on a MIPS floating point pipeline. Operand forwarding is implemented. [R indicate integer registers and F indicate floating point registers]. Find the clock cycle in which STOR instruction reaches MEM stage.

LOAD F4, 8(R2);

FMUL F0, F4, F2;

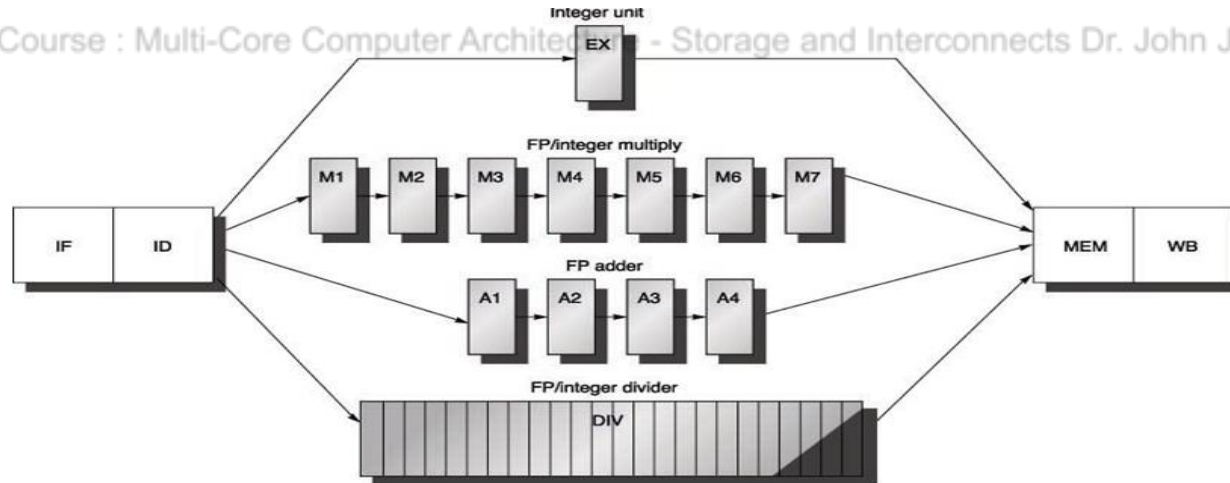
FADD F3, F0, F2;

STOR F3, 16(R3)

Tutorial Problem-4

- ❖ Consider the following instruction sequence executed on a MIPS floating point pipeline. Operand forwarding is implemented. [R indicate integer registers and F indicate floating point registers]. Find the clock cycle in which STOR instruction reaches MEM stage.

LOAD F4, 8(R2); FMUL F0, F4, F2; FADD F3, F0, F2; STOR F3, 16(R3)



Tutorial Problem-4

- ❖ Consider the following instruction sequence executed on a MIPS floating point pipeline. Operand forwarding is implemented. [R indicate integer registers and F indicate floating point registers]. Find the clock cycle in which STOR instruction reaches MEM stage.

LOAD F4, 8(R2); FMUL F0, F4, F2; FADD F3, F0, F2; STOR F3, 16(R3)

[illegible]

Tutorial Problem-5

- ❖ Consider two programs A and B that solve a given problem. A is scheduled to run on a processor P1 operating at 1 GHz and B is scheduled to run on processor P2 running at 1.4 GHz. A has total 5000 instructions, out of which 20% are branch instructions, 40% load store instructions and rest are ALU instructions. B is composed of 25% branch instructions. The number of load store instructions in B is twice the count of ALU instructions. Total instruction count of B is 6000. In both P1 and P2 branch instructions have an average CPI of 5 and ALU instructions have an average CPI of 1.2. Both the architectures differ in the CPI of load store instruction. They are 2 and 2.4 for P1 and P2 respectively. Given this setup which machine (A on P1 or B on P2) solves the problem faster, and by how much?

Tutorial Problem-5

A on P1 (1GHz → 1ns)	B on P2 (1.4 GHz→0.714ns)
IC=5000	IC=6000
Fraction BR: L/S: ALU = 20 : 40: 40	Fraction BR: L/S: ALU = 25 : 50: 25
CPI of BR: L/S: ALU = 5: 2 : 1.2	CPI of BR: L/S: ALU = 5: 2.4 : 1.2

**THANK
YOU!**



**FOR
YOUR
PRESENCE**

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